PRODUCT/PROCESS
CHANGE INFORMATION

PCI AMG/17/10616

Analog & MEMS Group (AMG)

Introduction of a new Lead-frame in ST Bouskoura for AMG products (Analog & MEMS Group) in SO8 package

WHAT:

Progressing on the activities related to our service continuous improvement, ST is glad to announce the introduction of a new Lead-frame format for AMG products in SO8 packages produced in our ST plant of Bouskoura.
This minor change consists in increasing the number of unit per lead-frame. The new Super High Density lead-frame will not affect the internal structure or the plating of the lead-frame.

Please find more information related to the change in the table here below

Material	Current process	Modified process	Comment
Diffusion location	No change		
Assembly location	ST Bouskoura	ST Bouskoura	No change
Molding compound	Sumitomo G700KC	Sumitomo G700KC	No change
Die attach	Ablestick 8601-S25	Ablestick 8601-S25	No change
Lead-frame	High Density (copper)	Super High density (copper)	No change package internal design
Wire	Copper 1 mil	Copper 1 mil	No change
Plating	Sn	Sn	No change

WHY:

This change will contribute to ST's continuous service improvement and ensure a consistent assembly process through all the SO production lines.

HOW:

The qualification program consists mainly of comparative electrical characterization and reliability tests.

You will find here after the qualification test plan which summarizes the various test methods and conditions that ST uses for this qualification program.

WHEN:

This Super High Density Lead-frame will be implemented in January 2018 in Bouskoura.

Marking and traceability:

Unless otherwise stated by customer's specific requirement, the traceability of the parts assembled with the new material set will be ensured by new internal sales type, date code and lot number.

The changes here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all the information reported on the relevant datasheets.
There is -as well- no change in the packing process or in the standard delivery quantities.

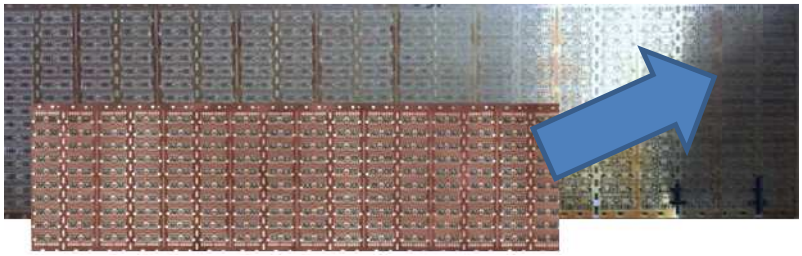
Shipments may start earlier with the customer's written agreement.

Reliability Report

Lead-frame format for SO8 in ST Bouskoura for AMG products

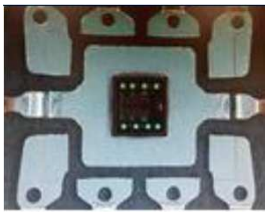
General Information on Test vehicles	
Product Line	*0393, V912, 0922, 0912, UY32, UW23, 16VA, UE27, 0303, U093, UQ18*
Product Description	Dual comparator, Dual op amp,
P/N	*LM2903DT, TV912IDT, TS922IDT, TS912IDT, TSX922IDT, ST3485, STM706, L6562, TSM103, L6561, PM881*
Product Group	*AMG*
Product division	*General Purpose Analog &RF, Industrial Power Conversion*
Package	*SO8*
Silicon Process technology	*Bipolar, HF5CMOS, HF2CMOS, HC1PA, HVG8A, BCD3S, HCMOS4, BCD2S, Bi-polar, BCD6, BCD6S*

Locations	
Wafer fab	*ST Singapore* *UMC* *ST Agrate* *ST Catania*
Assembly plant	*ST Bouskoura (Morocco)*
Reliability Lab	*ST Grenoble,* *ST Casteletto* *ST Agrate* *ST Catania* *ST Bouskoura*

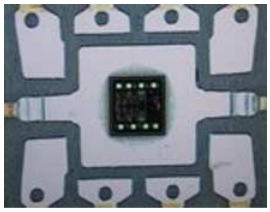


No change on the frame design inside the package

Current



New



Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods. This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

To qualify the Super High Density Lead-frame in SO8 package for products manufactured in ST Bouskoura.

3.2 Conclusion

Successful fulfillment of the qualification plan is required. It is stressed that reliability tests have to show that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests have to demonstrate the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

LM2903YDT

life.augmented

LM2903

Low-power dual voltage comparator

Datasheet - production data

N
DIP8
(plastic package)

D
SO8
(plastic micropackage)

P
TSSOP8
(thin shrink small outline package)

S
MiniSO8
(plastic micropackage)

DFN8 2x2 mm
(plastic micropackage)

Features

- Wide single supply voltage range or dual supplies +2 V to +36 V or ±1 V to ±18 V
- Very low supply current (0.4 mA) independent of supply voltage (1 mW/comparator at +5 V)
- Low input bias current: 25 nA typ.
- Low input offset current: ±5 nA typ.
- Input common-mode voltage range includes negative rail
- Low output saturation voltage: 250 mV typ. (I_O = 4 mA)
- Differential input voltage range equal to the supply voltage
- TTL, DTL, ECL, MOS, CMOS compatible outputs
- Automotive qualification

Related products

- See LM2903W for similar device with higher ESD performances
- See LM2903H for similar device with operating temperature up to 150 °C

Description

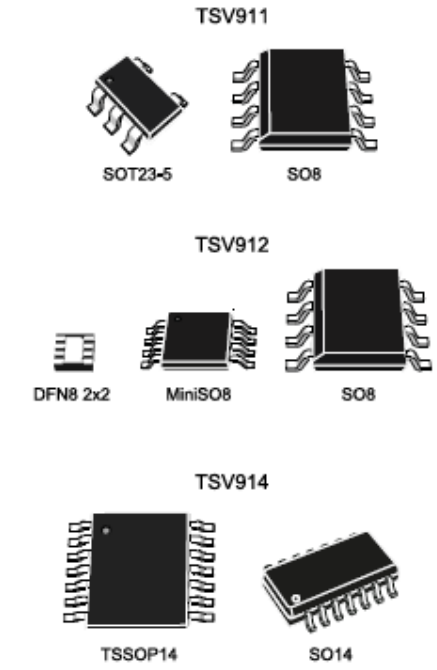
This device consists of two independent low-power voltage comparators designed specifically to operate from a single supply over a wide range of voltages. Operation from split power supplies is also possible.

In addition, the device has a unique characteristic in that the input common-mode voltage range includes the negative rail even though operated from a single power supply voltage.

TSV91x, TSV91xA

Single, dual, and quad rail-to-rail input/output 8 MHz operational amplifiers

Datasheet - production data



Features

- Rail-to-rail input and output
- Wide bandwidth
- Low power consumption: 820 µA typ
- Unity gain stability
- High output current: 35 mA
- Operating from 2.5 V to 5.5 V
- Low input bias current, 1 pA typ
- Low input offset voltage: 1.5 mV max (A grade)
- ESD internal protection ≥ 5 kV
- Latch-up immunity

Applications

- Battery-powered applications
- Portable devices
- Signal conditioning
- Active filtering
- Medical instrumentation
- Automotive applications

Related products

- See TSV99x, TSV99xA for higher gain bandwidth (not unity gain stable)

Description

The TSV91x operational amplifiers (op amps) offer low voltage operation and rail-to-rail input and output, as well as an excellent speed/power consumption ratio, providing an 8 MHz gain-bandwidth product while consuming only 1.1 mA maximum at 5 V. The op amps are unity gain stable and feature an ultra-low input bias current.

The devices are ideal for sensor interfaces, battery-supplied and portable applications, as well as active filtering.

Table 1: Device summary

Reference	Single	Dual	Quad
TSV91x	TSV911	TSV912	TSV914
TSV91xA (1)	TSV911A	TSV912A	TSV914A

Notes:

(1)Suffix "A" refers to enhanced V_{IO} performance

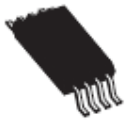
TS922, TS922A

Rail-to-rail, high output current, dual operational amplifier

Datasheet - production data

Flip-chip with backcoating

SO8



TSSOP8

Features

- Rail-to-rail input and output
- Low noise: 9 nV/√Hz
- Low distortion
- High output current: 80 mA (able to drive 32 Ω loads)
- High-speed: 4 MHz, 1 V/µs
- Operating from 2.7 to 12 V
- Low input offset voltage: 900 µV max. (TS922A)
- ESD internal protection: 2 kV
- Latch-up immunity
- Macromodel included in this specification
- Dual version available in Flip-chip package

Applications

- Headphone and servo amplifiers
- Sound cards, multimedia systems
- Line drivers, actuator drivers
- Mobile phones and portable equipment
- Instrumentation with low noise as key factor
- Piezoelectric speaker drivers

Description

TS922 and TS922A devices are rail-to-rail dual BiCMOS operational amplifiers optimized and fully specified for 3 V and 5 V operation. These devices have high output currents which allow low-load impedances to be driven.

Very low noise, low distortion, low offset, and a high output current capability make these devices an excellent choice for high quality, low voltage, or battery operated audio systems.

The devices are stable for capacitive loads up to 500 pF.

TS912, TS912A, TS912B

Rail-to-rail CMOS dual operational amplifier

Datasheet – production data

Features

- Rail-to-rail input and output voltage ranges
- Single (or dual) supply operation from 2.7 to 16 V
- Extremely low input bias current: 1 pA typ.
- Low input offset voltage: 2 mV max.
- Specified for 600 Ω and 100 Ω loads
- Low supply current: 200 µA/amplifier (V_{CC} = 3 V)
- Latch-up immunity
- ESD tolerance: 3 kV
- Spice macromodel included in this specification

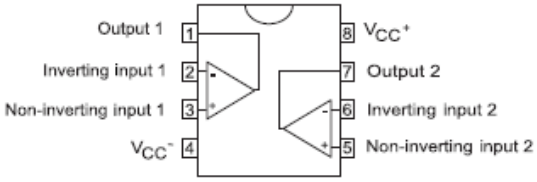
Related products

- See TS56x series for better accuracy and smaller packages

N
DIP8
(plastic package)

D
SO-8
(plastic micropackage)

Pin connections (top view)



Description

The TS912 device is a rail-to-rail CMOS dual operational amplifier designed to operate with a single or dual supply voltage.

The input voltage range V_{icm} includes the two supply rails V_{CC}^+ and V_{CC}^-.

The output reaches V_{CC}^- +30 mV, V_{CC}^+ -40 mV, with R_L = 10 kΩ and V_{CC}^- +300 mV, V_{CC}^+ -400 mV, with R_L = 600 Ω.

This product offers a broad supply voltage operating range from 2.7 to 16 V and a supply current of only 200 µA/amp. (V_{CC} = 3 V).

Source and sink output current capability is typically 40 mA (at V_{CC} = 3 V), fixed by an internal limitation circuit.

TL431
TL432

Programmable voltage reference

Datasheet – production data

Features

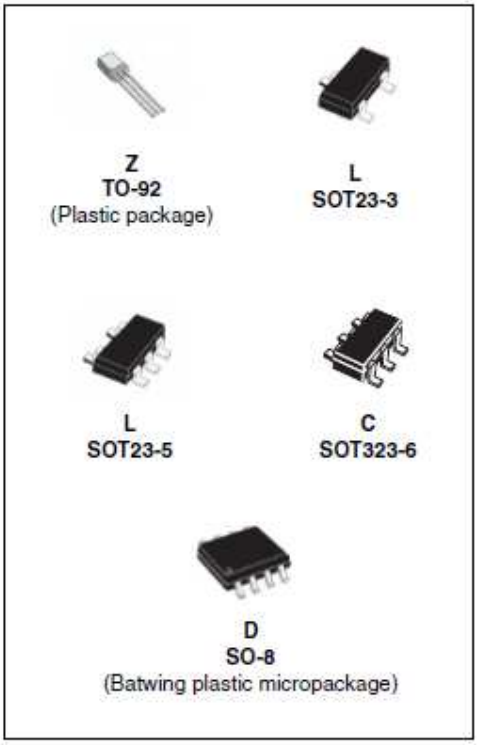
- Adjustable output voltage: 2.5 to 36 V
- Sink current capability: 1 to 100 mA
- Typical output impedance: 0.22 Ω
- 1% and 2% voltage precision
- Automotive temp. range - 40 °C to +125 °C

Applications

- Power supply
- Industrial
- Automotive

Description

The TL431 and TL432 are programmable shunt voltage references with guaranteed temperature stability over the entire operating temperature range. The device temperature range is extended for the automotive version from -40 °C up to +125 °C. The output voltage can be set to any value between 2.5 and 36 V with two external resistors. The TL431 and TL432 operate with a wide current range from 1 to 100 mA with a typical dynamic impedance of 0.22 Ω.



Z
TO-92
(Plastic package)

L
SOT23-3

L
SOT23-5

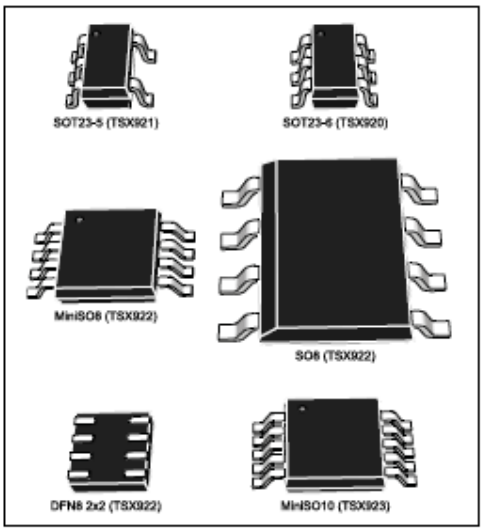
C
SOT323-6

D
SO-8
(Batwing plastic micropackage)

TSX920, TSX921, TSX922, TSX923

10 MHz rail-to-rail CMOS 16 V operational amplifiers

Datasheet - production data



Features

- Rail-to-rail input and output
- Wide supply voltage: 4 V - 16 V
- Gain bandwidth product: 10 MHz typ at 16 V
- Low power consumption: 2.8 mA typ per amplifier at 16 V
- Unity gain stable
- Low input bias current: 10 pA typ
- High tolerance to ESD: 4 kV HBM
- Extended temperature range: -40 °C to 125 °C
- Automotive qualification

Related products

- See the TSX5 series for low-power features
- See the TSX6 series for micro-power features
- See the TSX929 series for higher speeds
- See the TSV9 series for lower voltages

Applications

- Communications
- Process control
- Test equipment

Description

The TSX92x single and dual operational amplifiers (op amps) offer excellent AC characteristics such as 10 MHz gain bandwidth, 17 V/ms slew rate, and 0.0003 % THD+N. These features make the TSX92x family particularly well-adapted for communications, I/V amplifiers for ADCs, and active filtering applications.

Their rail-to-rail input and output capability, while operating on a wide supply voltage range of 4 V to 16 V, allows these devices to be used in a wide range of applications. Automotive qualification is available as these devices can be used in this market segment.

Shutdown mode is available on the single (TSX920) and dual (TSX923) versions enabling an important current consumption reduction while this function is active.

The TSX92x family is available in SMD packages featuring a high level of integration. The DFN8 package, used in the TSX922, with a typical size of 2x2 mm and a maximum height of 0.8 mm offers even greater package size reduction.

Table 1: Device summary

Op-amp version	With shutdown mode	Without shutdown mode
Single	TSX920	TSX921
Dual	TSX923	TSX922

ST3485EB, ST3485EC, ST3485EI, ST3485EIY

3.3 V powered, 15 kV ESD protected, up to 12 Mbps RS-485/ RS-422 transceiver

Datasheet - production data

SO8

Features

- ESD protection
  - ±15 kV IEC 61000-4-2 air discharge
  - ±8 kV IEC 61000-4-2 contact discharge
- Operate from a single 3.3 V supply - no charge pump required
- Interoperable with 5 V logic
- 1 µA low current shutdown mode max.
- Guaranteed 12 Mbps data rate
- -7 to 12 V common mode input voltage range
- Half duplex versions available
- Industry standard 75176 pinout
- Current limiting and thermal shutdown for driver overload protection
- Guaranteed high receiver output state for floating inputs with no signal present
- Allow up to 64 transceivers on the bus
- Available in SO8 package
- Automotive grade (ST3485EIY)

Description

The ST3485EB/EC/EI/EIY device is ±15 kV ESD protected, 3.3 V low power transceiver for RS-485 and RS-422 communications. The device contains one driver and one receiver in half duplex configuration.

The ST3485E device transmits and receives at a guaranteed data rate of at least 12 Mbps.

All transmitter outputs and receiver inputs are protected to ±15 kV IEC 61000-4-2 air discharge.

The driver is short-circuit current limited and is protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs into a high impedance state.

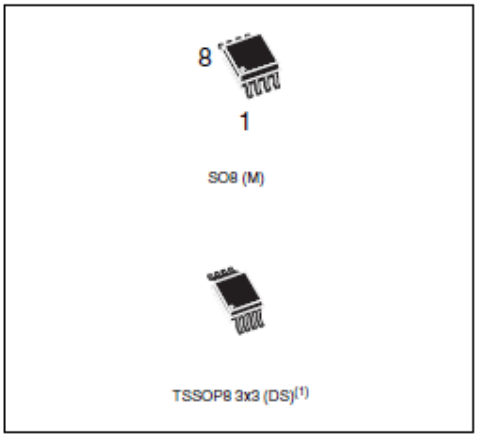
Table 1: Device summary

Order code	Temp. range	Package	Packing
ST3485ECDR	0 to 70 °C	SO8 (tape and reel)	2500 parts per reel
ST3485EBDR	-40 to 85 °C		
ST3485EIDT	-40 to 125 °C		
ST3485EIYDT			

STM705, STM706
STM707, STM708, STM813L

5 V supervisor

Datasheet - production data



1. Contact local ST sales office for availability.

- 200 ms (typ) t_{rec}
- Watchdog timer - 1.6 s (typ)
- Manual reset input ($\overline{MR}$)
- Power-fail comparator (PFI/$\overline{PFO}$)
- Low supply current - 40 µA (typ)
- Guaranteed $\overline{RST}$ (RST) assertion down to V_{CC} = 1.0 V
- Operating temperature:
  –40 °C to 85 °C (industrial grade) or
  –40 °C to 125 °C (automotive grade for the STM706 only)
- RoHS compliance
  – Lead-free components are compliant with the RoHS directive

Features

- 5 V operating voltage
- Precision V_{CC} monitor
  – STM705/707/813L
  – 4.50 V ≤ V_{RST} ≤ 4.75 V
  – STM706/708
  – 4.25 ≤ V_{RST} ≤ 4.50 V
- RST and $\overline{RST}$ outputs

Table 1. Device summary

	Watchdog input	Watchdog output(1)	Active-low $\overline{RST}$(1)	Active-high RST(1)	Manual reset input	Power-fail comparator
STM705	✓	✓	✓		✓	✓
STM706(2)	✓	✓	✓		✓	✓
STM707			✓	✓	✓	✓
STM708			✓	✓	✓	✓
STM813L	✓	✓		✓	✓	✓

1. Push-pull output
2. Automotive grade (-40 °C to 125 °C) option for the STM706 only.

L6562

TRANSITION-MODE PFC CONTROLLER

1 Features

- REALISED IN BCD TECHNOLOGY
- TRANSITION-MODE CONTROL OF PFC PRE-REGULATORS
- PROPRIETARY MULTIPLIER DESIGN FOR MINIMUM THD OF AC INPUT CURRENT
- VERY PRECISE ADJUSTABLE OUTPUT OVERVOLTAGE PROTECTION
- ULTRA-LOW (≤70µA) START-UP CURRENT
- LOW (≤4 mA) QUIESCENT CURRENT
- EXTENDED IC SUPPLY VOLTAGE RANGE
- ON-CHIP FILTER ON CURRENT SENSE
- DISABLE FUNCTION
- 1% (@ Tj = 25 °C) INTERNAL REFERENCE VOLTAGE
- -600/+800mA TOTEM POLE GATE DRIVER WITH UVLO PULL-DOWN AND VOLTAGE CLAMP
- DIP-8/SO-8 PACKAGES ECOPACK®

1.1 APPLICATIONS

- PFC PRE-REGULATORS FOR:
  - IEC61000-3-2 COMPLIANT SMPS (TV, DESKTOP PC, MONITOR) UP TO 300W
  - HI-END AC-DC ADAPTER/CHARGER
  - ENTRY LEVEL SERVER & WEB SERVER

Figure 1. Packages

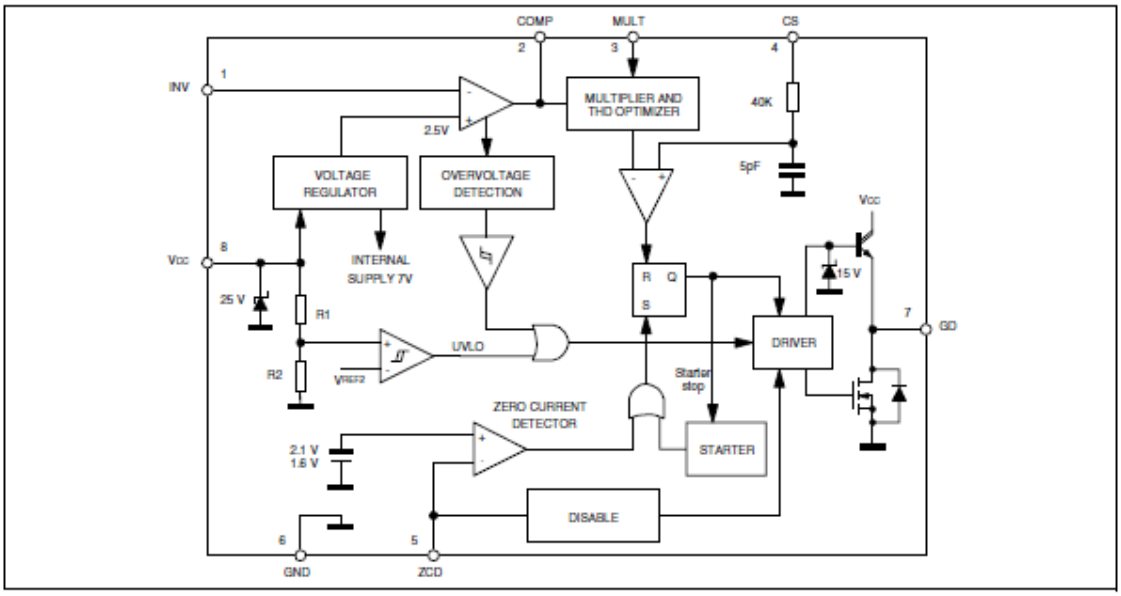
Table 1. Order Codes

Part Number	Package
L6562N	DIP-8
L6562D	SO-8
L6562DTR	Tape & Reel

2 Description

The L6562 is a current-mode PFC controller operating in Transition Mode (TM). Pin-to-pin compatible with the predecessor L6561, it offers improved performance.

Figure 2. Block Diagram



TSM103W

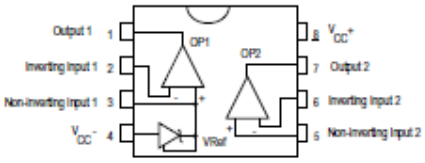
Dual Operational Amplifier and Voltage Reference

OPERATIONAL AMPLIFIER

- LOW INPUT OFFSET VOLTAGE : 0.5mV typ.
- LOW SUPPLY CURRENT : 350µA/op. (@ V_{cc} = 5V)
- MEDIUM BANDWIDTH (unity gain) : 0.9MHz
- LARGE OUTPUT VOLTAGE SWING : 0V to (V_{cc} - 1.5V)
- INPUT COMMON MODE VOLTAGE RANGE INCLUDES GROUND
- WIDE POWER SUPPLY RANGE : 3 to 32V ±1.5 TO ±16V
- 1.5kV ESD PROTECTION
- VOLTAGE REFERENCE
- FIXED OUTPUT VOLTAGE REFERENCE 2.5V
- ±0.4% OR ±0.7% VOLTAGE PRECISION
- SINK CURRENT CAPABILITY : 1 to 100mA
- TYPICAL OUTPUT IMPEDANCE : 0.2Ω

D
SO-8
(Plastic Micropackage)

PIN CONNECTIONS (top view)



DESCRIPTION

The TSM103W is a monolithic IC that includes one independent op-amp and another op-amp for which the non-inverting input is wired to a 2.5V fixed Voltage Reference. This device offers both space and cost savings in many applications such as power supply management or data acquisition systems.

ORDER CODE

Part Number	Temperature Range	Package	Packaging
TSM103WID	-40, +105°C	SO-8	Tube
TSM103WIDT			Tape & Ree
TSM103WAID			Tube
TSM103WAIDT			Tape & Reel

L6561

POWER FACTOR CORRECTOR

1 FEATURES

- VERY PRECISE ADJUSTABLE OUTPUT OVERVOLTAGE PROTECTION
- MICRO POWER START-UP CURRENT (50µA TYP.)
- VERY LOW OPERATING SUPPLY CURRENT(4mA TYP.)
- INTERNAL START-UP TIMER
- CURRENT SENSE FILTER ON CHIP
- DISABLE FUNCTION
- 1% PRECISION (@ T_j = 25°C) INTERNAL REFERENCE VOLTAGE
- TRANSITION MODE OPERATION
- TOTEM POLE OUTPUT CURRENT: ±400mA
- DIP-8/SO-8 PACKAGES

2 DESCRIPTION

L6561 is the improved version of the L6560 standard Power Factor Corrector. Fully compatible with the standard version, it has a superior performant multiplier making the device capable of working in wide input voltage range applications (from 85V to 265V) with an excellent THD. Furthermore the start up current has been reduced at few tens of mA and a disable function has been implemented on the ZCD pin, guaranteeing lower current consumption in stand by mode.

Figure 1. Packages

Table 1. Order Codes

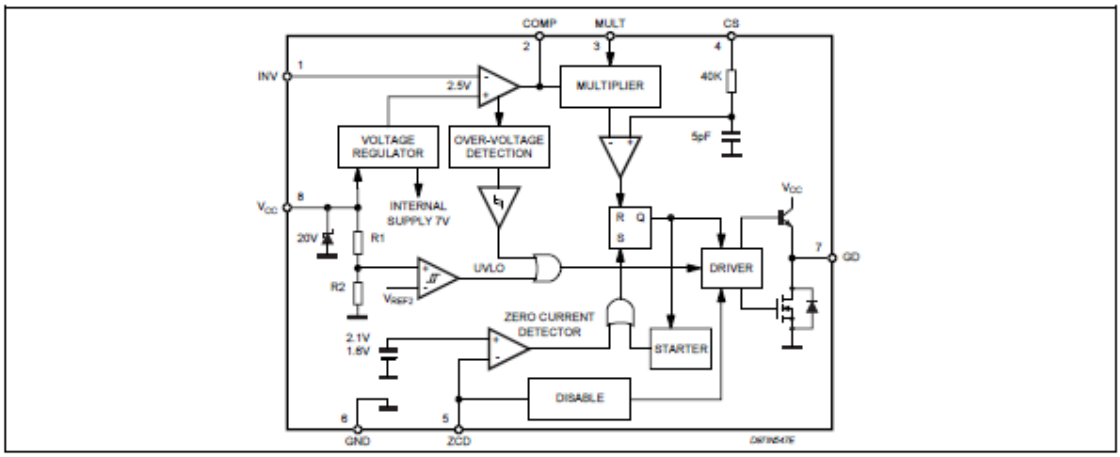
Part Number	Package
L6561	DIP-8
L6561D	SO-8
L6561D013TR	Tape & Reel

Realised in mixed BCD technology, the chip gives the following benefits:

- micro power start up current
- 1% precision internal reference voltage
- (Tj = 25°C)
- Soft Output Over Voltage Protection
- no need for external low pass filter on the current sense
- very low operating quiescent current minimises power dissipation

The totem pole output stage is capable of driving a Power MOS or IGBT with source and sink currents of ±400mA. The device is operating in transition mode and it is optimised for Electronic Lamp Ballast application, AC-DC adaptors and SMPS.

Figure 2. Block Diagram



4.2 Construction note

	P/N *LM2903DT*	P/N TSV912IDT	P/N TS922IDT	P/N TS912IDT	P/N TL431AIDT
Wafer/Die fab. information					
Wafer fab manufacturing location	ST Singapore	UMC taiwan	ST Singapore	ST Singapore	ST Singapore
Technology	Bipolar	HF5CMOS	HF2CMOS	HC1PA	HBIP40
Die finishing back side	RAW SILICON	RAW SILICON	RAW SILICON	RAW SILICON	RAW SILICON
Die size (microns)	950 x 870 µm	1100x1070µm	1720x1190µm	2600x1950	0,9x0,62
Bond pad metallization layers	AlSiCu	AlCu	AlSiCu	AlSi	AlSiCu
Passivation type	Nitride	Nitride	Nitride	PVAPOX+Nitride	PVAPOX+Nitride
Assembly information					
Assembly site	ST Bouskoura	ST Bouskoura	ST Bouskoura	ST Bouskoura	ST Bouskoura
Package description	SO8	SO8	SO8	SO8	SO8
Molding compound	EME G700KC	EME G700KC	EME G700KC	EME G700KC	EME G700KC
Frame material	Cu	Cu	Cu	Cu	Cu
Die attach process	Epoxy Glue	Epoxy Glue	Epoxy Glue	Epoxy Glue	Epoxy Glue
Die attach material	8601S-25	8601S-25	8601S-25	8601S-25	8601S-25
Wire bonding process	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding
Wires bonding materials/diameters	Cu 1 mil	Cu 1 mil	Cu 1 mil	Cu 1 mil	Cu 1 mil
Lead finishing process	electroplating	electroplating	electroplating	electroplating	electroplating
Lead finishing/bump solder material	Matte tin	Matte tin	Matte tin	Matte tin	Matte tin

	P/N TSX922IDT	P/N ST3485EIDT	P/N STM706M7F	P/N L6562	P/N TSM103
Wafer/Die fab. information					
Wafer fab manufacturing location	ST Agrate	ST Singapore	ST Singapore	ST Singapore	ST Singapore
Technology	HVG8A	BCD3S	HCMOS4	BCD2S	Bipolar
Die finishing back side	Raw silicon	Raw silicon	Raw silicon	CHROMIUM/NICKEL	Raw silicon
Die size (microns)	1700x1400µm²	1950x2720 µm²	1350x1510 µm²	1790x1870 µm²	1890x2120 µm²
Bond pad metallization layers	AlCu	AlSi	AlSiCu	AlSiCu	AlSiCu
Passivation type	HDP/TEOS/SiN/Polyimide	PVAPOX/ NITRIDE/POLYIMIDE	PVAPOX+Nitride	SiN/Poly	SiN/Poly
Assembly information					
Assembly site	ST Bouskoura	ST Bouskoura	ST Bouskoura	ST Bouskoura	ST Bouskoura
Package description	SO8	SO8	SO8	SO8	SO8
Molding compound	EME G700KC	EME G700KC	EME G700KC	EME G700KC	EME G700KC
Frame material	Cu	Cu	Cu	Cu	Cu
Die attach process	Epoxy Glue	Epoxy Glue	Epoxy Glue	Epoxy Glue	Epoxy Glue
Die attach material	8601S-25	8601S-25	8601S-25	8601S-25	8601S-25
Wire bonding process	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding
Wires bonding materials/diameters	Cu 1 mil	Cu 1 mil	Cu 1 mil	Cu 1 mil	Cu 1 mil
Lead finishing process	electroplating	electroplating	electroplating	electroplating	electroplating
Lead finishing/bump solder material	Matte tin	Matte tin	Matte tin	Matte tin	Matte tin

	P/N L6561D013TR
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Singapore
Technology	BCD6
Die finishing back side	CHROMIUM/NICKEL/GOLD
Die size (microns)	2590x2060 µm²
Bond pad metallization layers	AlSi
Passivation type	SiN
Assembly information	
Assembly site	ST Bouskoura
Package description	SO8
Molding compound	EME G700KC
Frame material	Cu
Die attach process	Epoxy Glue
Die attach material	8601S-25
Wire bonding process	Thermosonic ball bonding
Wires bonding materials/diameters	Cu 1 mil
Lead finishing process	electroplating
Lead finishing/bump solder material	Matte tin

5 TESTS RESULTS SUMMARY FOR SUPER HIGH DENSITY LEAD-FRAME

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	Bipolar/SO8	0393	CZ7410EH0G
2	HF5CMOS/SO8	V912	CZ7410F3RR
3	HF2CMOS / SO8	0922	CZ7420D203
4	HC1PA/SO8	0912	
5	HBIP40/SO8	0431	
6	HVG8A/SO8	UY32	
7	BCD3S/SO8	UW23	
8	HCMOS4/SO8	16VA	
9	BCD2S/SO8	UE27	
10	Bipolar/SO8	0303	
11	BCD6/SO8	U093	

5.2 Test plan and results summary

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS					Note
						Lot 1 0393	Lot 2 V912	Lot 3 0922	Lo4 0912	Lot5 0431	
HTB/ HTOL	N	JESD22 A-108	Ta = 150°C, BIAS		168 H	0/77		0/77			
					500 H	77		77			
					1000 H	77		77			
HTSL	N	JESD22 A-103	Ta = 150°C		168 H	0/77	0/77	0/77	77	45	
					500 H	0/77	0/77	0/77	77	45	
					1000 H	77	77	77	77	45	
Package Oriented Tests											
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times		Final	PASS	PASS	PASS	154	154	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		96 H 168H	0/77	0/77	0/77	77	77	
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		100 cy	0/77	0/77	0/77	77	77	
					200 cy	0/77	0/77	0/77	77	77	
					500 cy	0/77	0/77	0/77	77	77	
					1000cy	77	77	77	77	77	
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS		168 H	77					
					500 H	77					
					1000 H	77					

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS					Note
						Lot 6 UY32	Lot 7 UW23	Lot 8 16VA	Lo9 UE27	Lot10 0303	
HTB/ HTOL	N	JESD22 A-108	Ta = 150°C, BIAS		168 H						
					500 H						
					1000 H						
HTSL	N	JESD22 A-103	Ta = 150°C		168 H	77	77	77	45	45	
					500 H	77	77	77	45	45	
					1000 H	77	77	77	45	45	
Package Oriented Tests											
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times		Final	154	154	154	154	154	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		96 H 168H	77	77	77	77	77	
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		100 cy	77	77	77	77	77	
					200 cy	77	77	77	77	77	
					500 cy	77	77	77	77	77	
					1000cy	77	77	77	77	77	
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS		168 H						
					500 H						
					1000 H						

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS					Note
						Lot 11 U093					
HTB/ HTOL	N	JESD22 A-108	Ta = 150°C, BIAS		168 H						
					500 H						
					1000 H						
HTSL	N	JESD22 A-103	Ta = 150°C		168 H	77					
					500 H	77					
					1000 H	77					
Package Oriented Tests											
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times		Final	154					
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		96 H 168H	77					
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		100 cy	77					
					200 cy	77					
					500 cy	77					
					1000cy	77					
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS		168 H						
					500 H						
					1000 H						

Just for your reference, please find here below the results of the ***Current High density Lead-frame*** (with the same material set)

	P/N *LM2903YDT*	P/N *LM2901YDT*	P/N *TL084IYDT*	P/N ST3485EIYDT	P/N TS924IDT
Wafer/Die fab. information					
Wafer fab manufacturing location	ST Singapore	ST Singapore	ST Singapore	ST Singapore	ST Singapore
Technology	Bipolar	Bipolar	JFet	BCD3S	HF2CMOS
Die finishing back side	RAW SILICON	RAW SILICON	RAW SILICON	RAW SILICON	RAW SILICON
Die size (microns)	950 x 870 µm	1370x1270	2480 x 1460	1950x2720	1980x2450
Bond pad metallization layers	AlSiCu	AlSiCu	AlSiCu	AlSi	AlSiCu
Passivation type	Nitride	Nitride	P-VAPOX/NITRIDE	P-VAPOX/NITRIDE/POLYIMIDE	P-VAPOX/NITRIDE
Wafer Testing (EWS) information					
Electrical testing manufacturing location	ST Singapore	ST Singapore	ST Singapore	ST Singapore	ST Singapore
Tester	ASL1K	ASL1K	ASL1K	ASL1K	ASL1K
Assembly information					
Assembly site	ST Bouskoura	ST Bouskoura	ST Bouskoura	ST Bouskoura	ST Bouskoura
Package description	SO8	SO14	SO14	SO8	SO14
Molding compound	EME G700KC	EME G700KC	EME G700KC	EME G700KC	EME G700KC
Frame material	Cu	Cu	Cu	Cu	Cu
Die attach process	Epoxy Glue	Epoxy Glue	Epoxy Glue	Epoxy Glue	Epoxy Glue
Die attach material	8601S-25	8601S-25	8601S-25	8601S-25	8601S-25
Wire bonding process	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding
Wires bonding materials/diameters	Cu 1 mil	Cu 1 mil	Cu 1 mil	Cu 1 mil	Cu 1 mil
Lead finishing process	electroplating	electroplating	electroplating	electroplating	electroplating
Lead finishing/bump solder material	Matte tin	Matte tin	Matte tin	Matte tin	Matte tin
Final testing information					
Testing location	ST Bouskoura	ST Bouskoura	ST Bouskoura	ST Bouskoura	ST Bouskoura
Tester	ASL1K	ASL1K	ASL1K	ASL1K	ASL1K

	P/N *TSX3704IYDT*	P/N *TSX3702IYDT*	P/N STM706YM7F	P/N MC33079YDT	P/N TS912IYDT	P/N TSV912IYDT
Wafer/Die fab. information						
Wafer fab manufacturing location	ST Agrate	ST Agrate	ST Singapore	ST Singapore	ST Singapore	UMC
Technology	HVG8A	HVG8A	HCMOS4	Bipolar	HC1PA	HF5CMOS
Die finishing back side	RAW SILICON	RAW SILICON	RAW SILICON	RAW SILICON	RAW SILICON	RAW SILICON
Die size (microns)	1830x1440 µm	1018x1238 µm	1350 x1510µm	3230x1950µm	2600x1950µm	1100x1070µm
Bond pad metallization layers	AlCu	AlCu	AlSiCu	AlSiCu	AlSi	AlCu
Passivation type	HDP/TEOS/SiN/Polyimide	HDP/TEOS/SiN/Polyimide	PSG+Silicon Nitride+Polyimide	Nitride	PVAPOX+Nitride	Nitride
Wafer Testing (EWS) information						
Electrical testing manufacturing location	ST Singapore	ST Singapore	ST Singapore	ST Singapore	ST Singapore	ST Singapore
Tester	ASL1K	ASL1K	ASL1K	ASL1K	ASL1K	ASL1K
Assembly information						
Assembly site	ST Bouskoura	ST Bouskoura	ST Bouskoura	ST Bouskoura	ST Bouskoura	ST Bouskoura
Package description	SO14	SO14	SO8	SO14	SO8	SO8
Molding compound	EME G700KC	EME G700KC	EME G700KC	EME G700KC	EME G700KC	EME G700KC
Frame material	Cu	Cu	Cu	Cu	Cu	Cu
Die attach process	Epoxy Glue	Epoxy Glue	Epoxy Glue	Epoxy Glue	Epoxy Glue	Epoxy Glue
Die attach material	8601S-25	8601S-25	8601S-25	8601S-25	8601S-25	8601S-25
Wire bonding process	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding
Wires bonding materials/diameters	Cu 1 mil	Cu 1 mil	Cu 1 mil	Cu 1 mil	Cu 1 mil	Cu 1 mil
Lead finishing process	electroplating	electroplating	electroplating	electroplating	electroplating	electroplating
Lead finishing/bump solder material	Matte tin	Matte tin	Matte tin	Matte tin	Matte tin	Matte tin
Final testing information						
Testing location	ST Bouskoura	ST Bouskoura	ST Bouskoura	ST Bouskoura	ST Bouskoura	ST Bouskoura

6 TESTS RESULTS SUMMARY ON HIGH DENSITY LINE

(*CURRENT LEAD-FRAME)*

6.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	Bipolar/SO8	0393	CZ53005LRP CZ53005LRN CZ53005LRQ CZ53005LRR CZ53005LRM CZ53005LRL
2	BCD3S/SO8	UW23	CZ5430CN
3	HVG8A/SO8	UY18	CZ537088RM
4	HCMOS4/SO8	16VA	CZ53607S
5	HF5CMOS/SO8	V912	CZ544OC1RR

6.2 Test plan and results summary

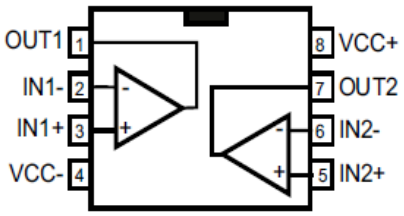
Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS					Note
						Lot 1 0393	Lot 2 UW23	Lot 3 UY18	Lot 4 16VA	Lot5 V912	
HTB/ HTOL	N	JESD22 A-108	Ta = 150°C, BIAS		168 H	0/78	0/77*		0/77*	0/77*	* Tj=125°C
					500 H	0/78	0/77*		0/77*	0/77*	
					1000 H	0/78	0/77*		0/77*	0/77*	
ELFR	N	JESD22 A-008	Ta = 125°C, BIAS			0/450		0/450		0/450	
HTSL	N	JESD22 A-103	Ta = 150°C		168 H	6X0/77	0/45	0/77	0/45		
					500 H	6X0/77	0/45	0/77	0/45		
					1000 H	6X0/77	0/45		0/45		
					2000H						
Package Oriented Tests											
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times		Final	PASS	PASS	PASS	PASS		
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		96 H 168H	6x0/77	0/77 0/77		0/77 0/77		
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		100 cy	6x0/77	0/77	0/77	0/77		
					200 cy	6x0/77	0/77	0/77	0/77		
					500 cy	6x0/77	0/77	0/77	0/77		
					1000cy	6x0/77			0/77		
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS		168 H		0/77		0/77		
					500 H		0/77		0/77		
					1000 H		0/77		0/77		
Other Tests											
ESD	N	AEC Q101-001, 002 and 005	CDM								
						0/3			0/3		
SD	N		After ageing 8h and 16h			Pass	Pass		PASS		

7 ANNEXES

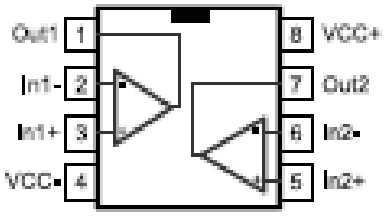
7.1 Device details

7.1.1 Pin connection

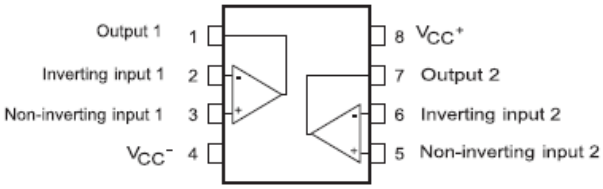
LM2903



V912

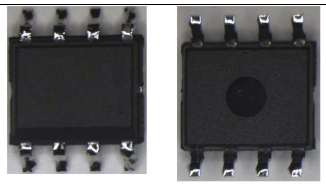
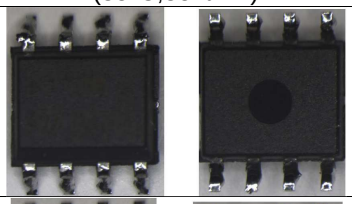
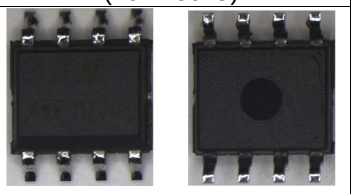
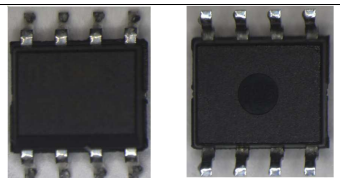
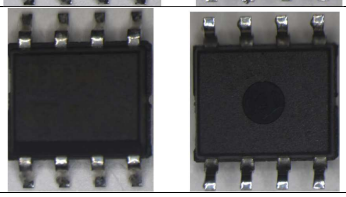
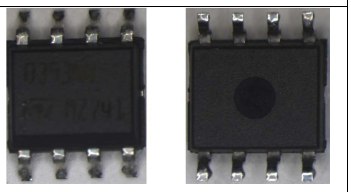


0922

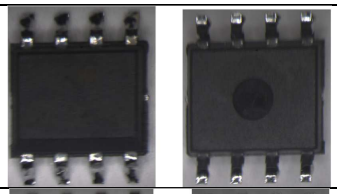
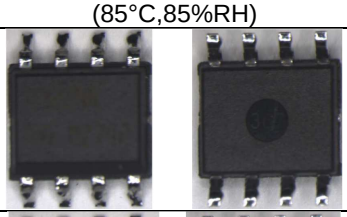
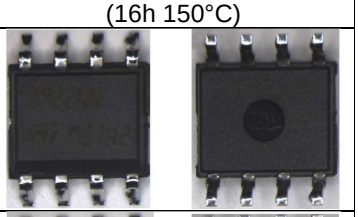
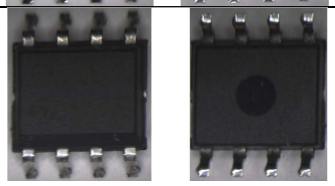
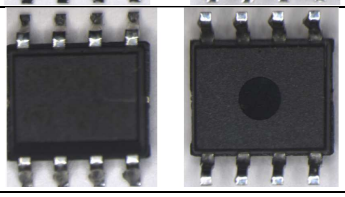
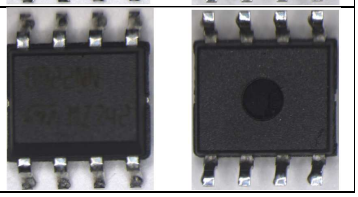


7.2 Construction analysis

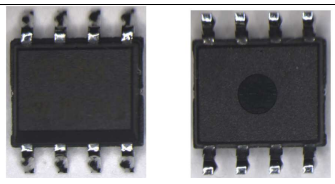
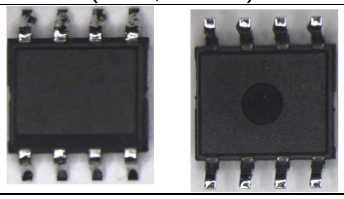
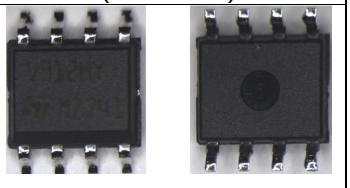
Solderability

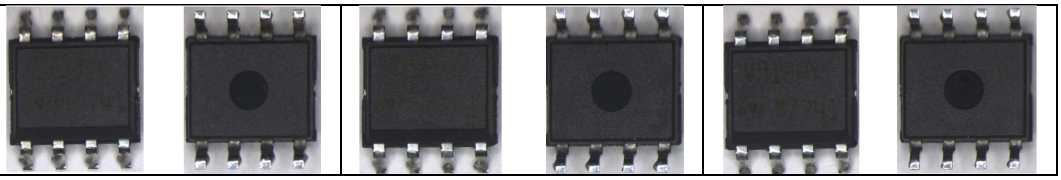
Dice 0393	T0	After 8h steam ageing (85°C,85%RH)	After dry ageing (16h 150°C)
SnPb bath			
SnAgCu bath			

Conclusion no reject (coverage >95%)

Dice 0922	T0	After 8h steam ageing (85°C,85%RH)	After dry ageing (16h 150°C)
SnPb bath			
SnAgCu bath			

Conclusion no reject (coverage >95%)

Dice V912	T0	After 8h steam ageing (85°C,85%RH)	After dry ageing (16h 150°C)
SnPb bath			

SnAgCu bath	

Conclusion no reject (coverage >95%)

Ball shear test

Value in g.

Dice	0393	V912	0922
Average	33.59	32.16	33.39
Max	38.86	34.68	35.26
Min	29.12	27.57	31.16
Cpk	1.78	2.51	2.72

Pull test

Value in g.

Dice	0393	V912	0922
Average	14.10	15.28	14.91
Max	15.34	16.95	16.42
Min	12.64	13.98	13.24
Cpk	4.71	4.10	5.04

7.3 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operating Life **HTB** High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTRB High Temperature Reverse Bias **HTFB / HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
ELFR Early Life Failure Rate	The device is stressed in biased conditions at the max junction temperature.	To evaluate the defects inducing failure in early life.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.

Test name	Description	Purpose
TF / IOL Thermal Fatigue / Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. CBM: Charged Device Model HBM: Human Body Model MM: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up.